A 0.82V Supply and 23.4 ppm/^{0}C Current Mirror Assisted Bandgap Reference

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***Abstract*— Traditional BGR circuits require a 1.05V supply due to the V_{BE} of the BJT. Deep submicron CMOS technologies are limiting the supply voltage to less than 940mV. Hence there is a strong motivation to design them at lower supply voltages. The supply voltage limitation in conventional BGR is described qualitatively in this paper. Further, a current mirror-assisted technique has been proposed to enable BGR operational at 0.82V supply. A prototype was developed in 65nm TSMC CMOS technology and post-layout simulation results were performed. A self-bias opamp has been exploited to minimize the systematic offset. Proposed BGR targeted at 450mV works from 0.82-1.05V supply without having any degradation in the performance while keeping the integrated noise of 15.2µV and accuracy of 23.4ppm/^{0}C. Further, the circuit consumes 21µW of power and occupies 73*32µm^{2}silicon area.**

Keywords—BGR, noise, Low voltage, PSRR, self-bias phase-margin.

I. Introduction

Analog and mixed-signal designs are getting a lot of traction these days because of the sensors domination in the modern era. All these sensor's require highly accurate and resolution ADC (12-Bit and 10Ms/s) [3] for typical applications. For a 1.2V supply, a 10Bit ADC requires 0.1% accurate reference voltage, which demands <0.1% bandgap reference. Historically BGR's were popular since 1980[1][2] in the 5V supply technology. They have started with the BJT-based opamps and PTAT generation circuitry. Unfortunately, this proposal can provide only a fixed output 1.23V (close to the silicon bandgap energy). [4] Bamba proposed a current-mode bandgap, where the o/p voltage can be any voltage, that's why it is called a sub-1V design. But this won't perform well under 1V supply. And also this has multiple operating problems, hence prone to failures. [7] proposed a mixed-mode BGR, which will work better than existing from the performance point of view, but it will also have issues under-1V supply. [5] proposed an opamp less BGR, which uses a self-bias common gate-based amplifier. This consumes very low power and uses less resistance value but this also requires more voltage. [6] proposes a state high accuracy bandgap by exploiting the BJT base driven circuitry, and it achieves 19.8ppm/0C temperature coefficient. Unfortunately, this requires 1-point trimming, and also several opamps are required instead of one in the conventional one.

The rest of the paper has been organized as follows. Section II analyses the Current mode bandgap reference and its voltage limitations. section III explains the limitations of the traditional ckt. section IV explains the concept of the proposed technique and finally, section V summarizes the simulation results.

II. Conventional Bandgap Reference

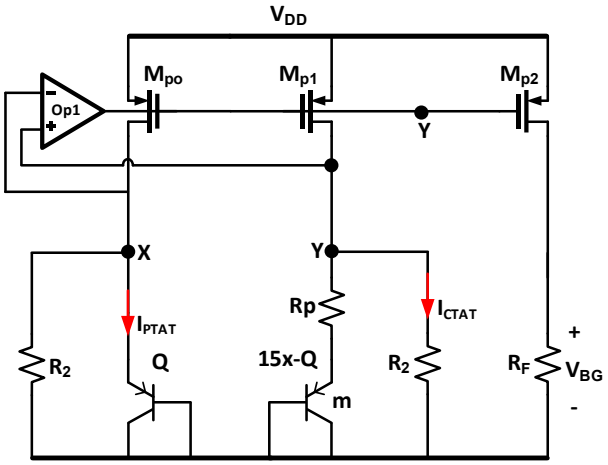

Fig. 1. Current mode Bandgap Schematic.

The main principle of bandgap reference is the scaled summation of CTAT and PTAT voltages. Base to Emitter voltage (VBE) of a BJT can be expressed as follows. Where I_C,I_S are the collector and saturation current.

$$V_{BE} = V_T \ln\left(1 + \frac{I_C}{I_S}\right) \quad (1)$$

The V_{BE} has a negative temperature coefficient (≈-1.6mv/^{0}C), hence it can be used as CTAT voltage. The delta VBE of two BJT voltages with different current densities has PTAT nature as shown in equation (2), where n is the current density ratio of the two BJT's.

$$\delta V_{BE} = V_T \ln n \quad (2)$$

Fig:1 shows the popular current mode BGR, which works on the principle of adding PTAT and CTAT currents. Resistor

R_P carries PTAT current because the voltage across the resistor is PTAT voltage, which is given by equation (3).

$$I_{RP} = \frac{V_T \ln n}{R_P} \quad (3)$$

The voltage across resistance R_2 is V_{BE} of the BJT, hence it will carry CTAT nature current, which is expressed as (4).

$$I_{R2} = \frac{V_{BE1}}{R_2} \quad (4)$$

The summation of these two currents will flow through M_{p0}, which can be adjusted to have zero temp coefficient. Equation (5) gives the o/p voltage.

$$V_{BG} = \frac{R_F}{R_2}\left[\frac{R_2}{R_P} V_T \ln n + V_{BE1}\right] \quad (5)$$

Generally, V_{BE1} temperature coefficient is -1.6mv/^{0}C and for a typical choice of n=8 (for the layout complexity and matching purpose), the R_2/R_p ratio needs to be around 9.23, to keep the o/p voltage temperature coefficient close to zero. Also (5) reveals that o/p voltage will be scaled by R_f/R_2 ratio, hence o/p can be sub-1V voltage, which is the great advantage of the Bamba bandgap reference[8]. However, this has several disadvantages. 1. For 1uA bandgap core current, R_1 will be 51KΩ and R_2 will be in the order of 470kΩ, in this proposal two such resistors are needed. The recent study shows that these two resistors will occupy 92% of the bandgap area [10]. The banba bandgap circuit has multiple operating point as explained in [17].The minimum supply voltage will be around 1V; hence sub 1V supply operation won't be possible as explained in section-2.

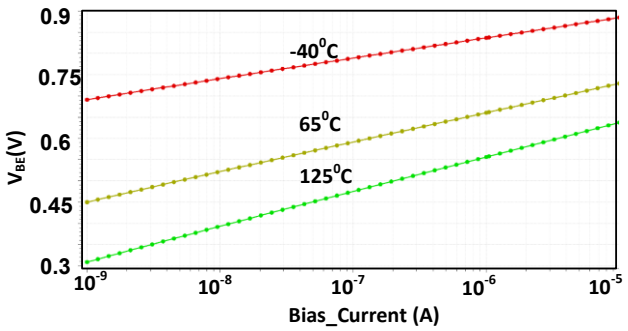

Fig. 2. BJT V_{BE} versus Bias current..

III. Design Techniques.

To come up with a low voltage design solution, one needs to understand what are the different headroom contributors. From fig:1, it is clear that we need to maintain V_{dsat} voltage across the M_{p0} to keep that device in the saturation region and V_{be} across the BJT. For a given technology V_{dsat} can't be reduced to less than 50mV, without sacrificing the PSRR and supply regulation parameters. The V_{BE} of the BJT will be in between the 450-950mV wrt to the temperature. Hence the min required supply voltage is 1000mV at the lower temperature (-40^{0}C). Could we do anything to decrease the V_{BE}, such that the bandgap would work with the lower power supply voltage. Fundamentally the diode voltage will scale with the current in a log-fashion, hence decreasing the bias current would decrease the voltage. Fig:2 shows the diode voltage versus bias current for different temperatures.

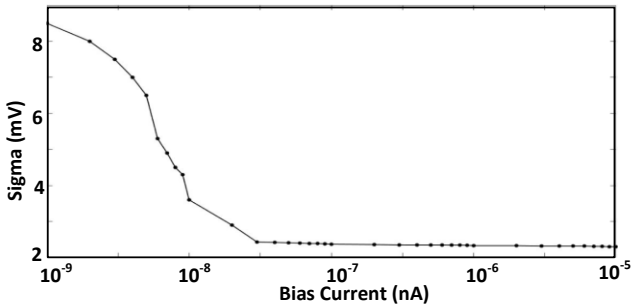

Fig. 3. Sigma of V_{BE} versus Bias current..

It shows V_{BE} could be as low as 690mV with 1nA current, with this operating current, it is possible to design BGR with 740mV supply voltage (assuming 50mV for the current source). But are any other parameters getting compromised with such low bias current? One major issue with parasitic PNP devices is extremely poor current gain (β), which leads to high base current and hence less collector current. Most importantly β is strongly depended on the current, which will lead to the variation wrt temperature as well[10][9]. The sigma of the V_{BE} can also be very sensitive at such a lower current. Fig:3 shows the Monte-Carlo results wrt to the bias current at higher temperature (-125^{0}C). It depicts that when the current less than 15nA, the sigma is increasing significantly, so the accuracy of the BGR will be compromised. Hence from the BJT point of view always there will be an optimal bias current which will minimize the V_{BE} and minimum sigma of V_{BE}.

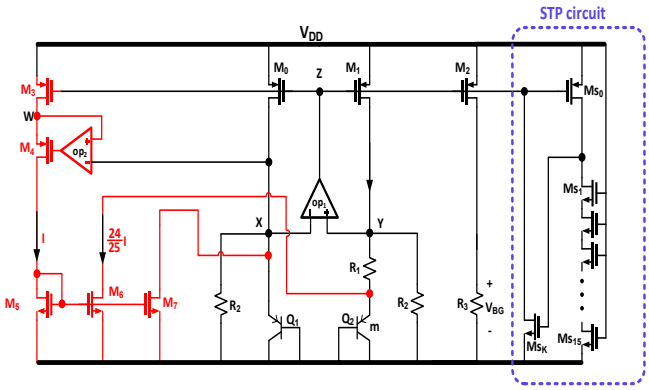

Fig. 4. Proposed design.

Now the point is would it be possible to design the entire bandgap core with such a low current? The first is the area will be blown up because of the following reason. From equation (3), it is clear that for a given BJT ratio (n), the resistor value is very high. For example, when n=8, the PTAT resistance (R_p) will 189kΩ, which makes R_2 is in the order of

mega–ohms. Also from [11][12], MOS current sources need biased at much higher currents inorder to keep them in saturation and minimizes the current mismatch. So the best way to design BGR is to use very little current for BJT and high current for current sources.

IV. PROPOSED TECHNIQUE

The main idea behind the proposal is to subtract the fraction of the PTAT, such that BJT will carry very less current. Fig:4 shows the proposed solution to realize the low voltage bandgap reference. Q_1,Q_2,R_1,M_0,M_1 forms the bandgap core. Here M_3 will sense the BGR core current and generate 24/25th fraction of the current through M_5-M_6, M_7 current mirrors. So the current flowing through the Q_1,Q_2 will be 1/25th of the M_0,M_1 currents. In the present example, 1µA has been used for the PMOS current sources and 40nA will be flowing through the Q_1, Q_2. Any mismatch in the current subtraction current mirror will reflect as an offset and compromises the bandgap accuracy[13]. M_0,M_1 drain potential will be similar to the CTAT voltage, hence to minimize the channel length modulation induced current error, op_2 opamp will drive the cascade M_4 gate such that node w potential is exactly equal to x&y. The o/p voltage can be expressed as (6), very similar to the conventional one.

$$V_{BG} = \frac{R_3}{R_2}\left[\frac{R_2}{R_1} V_T \ln n + V_{BE1}\right] \quad (6)$$

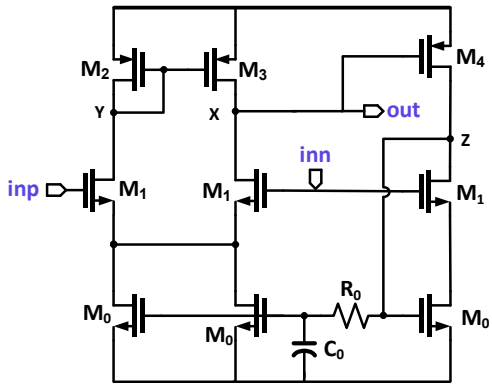

Fig. 5. O/p voltage vs temperature across PVT.

The opamp (op1) will play a significant role in the circuit performance, because its offset will appear at the o/p with a large conversion gain as expressed as (7), where v_{os} is the opamp offset[18]. The offset itself is not a big issue but its temp coefficient will compromise the o/p accuracy. This explains that choosing max n value will reduce the R_2/R_1, which interns improve the o/p temperature coefficient.

$$V_{BG-os} = \left(1 + \frac{R_2}{R_1}\right) V_{os} \quad (7)$$

Fig:5 shows the self-bias opamp used in the present design [15]. Mainly this opamp's tail current will track with the PTAT current flowing through the bandgap core circuit. M_0, M_1,M_2,M_3 form the traditional differential pair and node-x will drive the bandgap. M4 will sense the opamp current and adjust the tail current such that opamp and bandgap core current will be tracked. The Self-bias loop has to be much slower than the actual loop, hence used 50KHz low pass filter (R_o-C_o) from the M_{0b} to M_o transistor gate. Unfortunately, self-bias needs start up circuit too, but the BGR start-up circuit can be used to kick this opamp as well. A simple Lag compensation has been used to stabilize the opamp. A series RC circuit (600Ω-17.3pF) was connected from the opamp o/p to the supply. This style of compensation shows better PSRR performance compared to miller as described [14].

V. SIMULATION RESULTS.

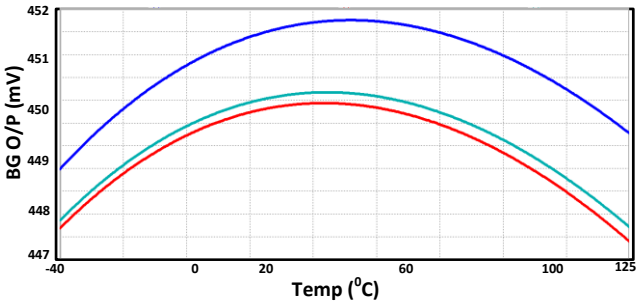

Fig. 6. O/p voltage vs temperature across PVT.

The proposed technique has been implemented in 65nm CMOS technology and post-layout simulations have been carried out. Fig:6 shows the temperature drift of the o/p wrt Process, voltage corners. The max drift ~3.9mV, means 23.4ppm/^{0}C temp-co.

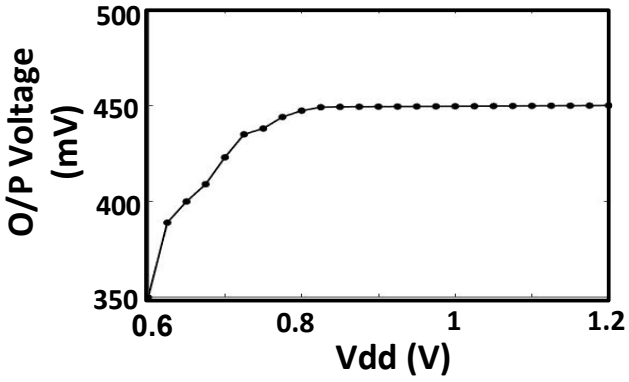

Fig. 7. Supply Regulation

To find the absolute min operating supply voltage, v_{dd} has been swept from 600mV to 1200mV, the o/p stays with-in 0.2% for the vdd above 820mV, any vdd less than this has significant change in o/p, because it is limited by the M_3,M_4,M_5 bias branch in fig:4 and opamp (op_1) o/p devices moving out of saturation region. Whereas the traditional Bamba architecture's minimum operating V_{DD} ~1V. Fig:8 shows the noise spectral density at the o/p of the BGR, it shows -150dB at 1KHz and 450KHz flicker noise corner frequency. The integrated RMS noise ~15.8µV across the full

frequency band. Fig:9 shows the simulated PSRR, which displays -58dB within the loop bandwidth and reaches -18.7dB at 13KHz. The low-frequency psrr is attributed to ~60dB loop gain and high-frequency roll of because of the decap dominated o/p impedance[16].

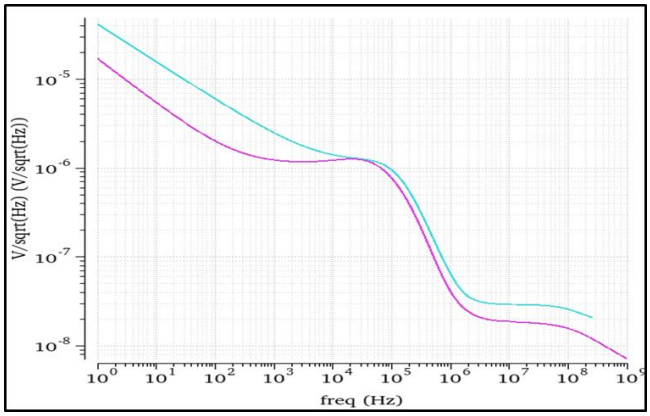

Fig. 8. Noise in Worst corner

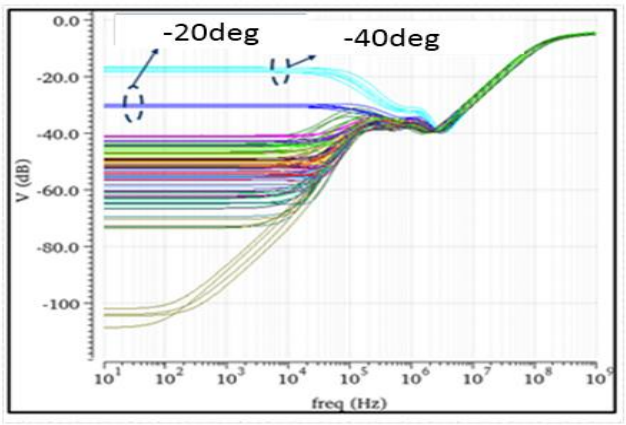

Fig. 9. Power supply rejection ratio (PSRR)

This 3.6dB better than the state of art, mostly because of the wide loop bandwidth and also this is the reason why miller comp has been avoided. Fig:10 shows the 500 point Monte Carlo simulation results, resulting the sigma of 720µV, which is 0.16% accuracy. Fig:11 depicts the layout of the proposal, which occupies 2336µm^2. Mainly it is drawn based on matching and low dc drop concern. Used inter-digitization techniques for current mirror and common centroid technique for both opamp differential pairs. In this proposal matching of the M_6,M_7 are extremely important. Care has been taken to avoid LOD and well proximity effect by keeping the devices far from nwell[16].

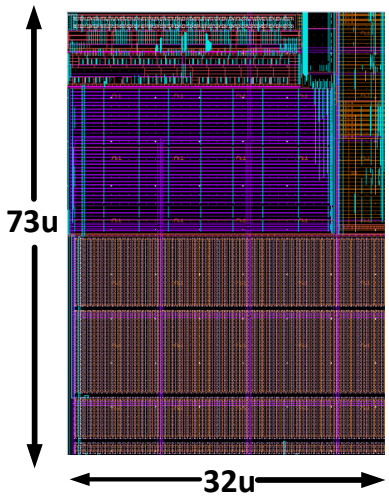

Fig. 10. The layout of the proposed circuit.

VI. Conclusion

In this paper, a state of the art low voltage (0.82V) bandgap reference has been proposed with 22ppm/^{0}C temperature coefficient. In-detailed analysis has been given to find the bottlenecks for the low voltage designs and exploited a current subtraction technique to achieve this.

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